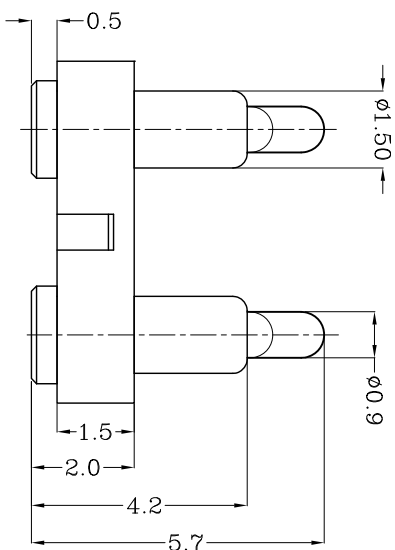
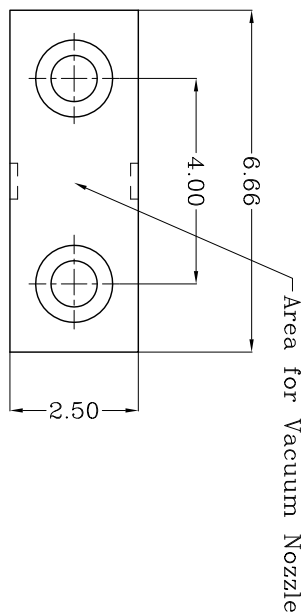


Recommended PCB Layout

USED ON

Plating Plunger: Min 0.4µm Au over 1.4µm Ni
Plating Body: Min 0.1µm Au over 1.4µm .

	new	08//07/14
LTR	REVISION RECORD	APVD DATE

DIMENSIONS IN MM TOLERANCES UNLESS OTHER SPECIFIED		MATL		HT TR	—	FIN	—	
0	= ±	DWN		APVD				
0.0	= ±0.15	qin		lansing		Top-Link		
0.00	= ±0.10	CHK		REL		Electronics L ttd		
0.000	= ±	Jlm				<i>Top-Link Electronics</i>		
ANGLE: ±1°								
SURF TEXTURE: 32/ 		BATTERY POGO CONNECTOR						
REMOVE BURRS, BREAK SHARP EDGES R0.05 MAX		2 POSITIONS PGC-15-5-7-R-2P-4.0PH						
DO NOT SCALE PRINT		SCALE	A4	DWG NO.	C-100357	SHEET 1 OF 1	REV A	

100357-2
PART NUMBER